UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,651	07/31/2003	Octavian Florescu	020556	3569

23696 7590 05/12/2004

Qualcomm Incorporated
Patents Department
5775 Morehouse Drive
San Diego, CA 92121-1714

EXAMINER	
NGUYEN, LINH M	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No.	Applicant(s)	
	10/632,651	FLORESCU, OCTAVIAN	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1-8,11-15,17-19,21-24,27-31 and 33* is/are rejected.

7)☒ Claim(s) *9,10,16,25,26 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Pri rity under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/31/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-33 are presented in the instant application according to the Applicant's filing on 07/31/2003.

Claim Objections/Minor Informalities

1. Claims 2 and 14 are objected to because of the following informalities:

Line 7, insert -- of -- in front of "an" (second occurrence).

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 18 and 19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 18 recites the limitation "the first propagation delay" in "the first propagation delay is a clock-to-Q propagation". There is insufficient antecedent basis for this limitation in the claim.

Furthermore, regarding claim 18, the limitation "the first propagation delay is a clock-to-Q propagation" renders the claim indefinite since there is no connection between this limitation and independent 14, which it depends on.

With respect to claim 19, the limitation "an asynchronous reset feature to permit asynchronous reset of the output independently of a clock signal generated by the clock

source" renders the claim indefinite since there is no connection between this limitation and independent 14, which it depends on.

Clarification is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, 5, 13, 28 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Oosera et al. (JP. Patent No. JP409046189A).

With respect to claims 1 and 28, Oosera et al. discloses, in Figure 1, a clock distribution circuit ant a corresponding method comprising a) a clock source [10] to generate a clock signal [Ai]; b) a clock divider [11] to divide the clock signal and produce a divided clock signal, and including a flip-flop [D flip-flop] that introduces a first propagation delay to the divided clock signal; and c) a delay matching circuit [12] to distribute the clock signal, and to introduce a second propagation delay to the clock signal, the second propagation delay substantially matching the first propagation delay introduced in the divided clock signal by the flip-flop.

With respect to claim 3, Oosera et al. discloses, in Figure 1, that the delay matching circuit substantially mimics current signal and current sourcing characteristics of the flip-flop.

With respect to claims 5 and 30, Oosera et al. discloses, in Figure 1, that the first propagation delay is a clock-to-Q propagation delay.

With respect to claim 13, Oosera et al. discloses, in Figure 1, that clock divider includes a first asynchronous reset feature [CD of 11] and the delay matching circuit includes a second asynchronous reset feature [CD of 12] that mimics operation of the first asynchronous reset feature.

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

7. Claims 14-15, 17 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen et al. (U.S. Patent No. 6,477,592).

With respect to claim 14, Chen et al. discloses, in Figure 7, a delay matching circuit comprising a) a multiplexer coupled to a clock source [not shown, which generates clock signal CLK2]; b) transmission gates [(66,68,70,72); (74,76,78,80)] within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop; c) inputs [D, Db] coupled to the multiplexer to substantially mimic characteristics of a master output driver of the

flip-flop; and d) an output coupled to the multiplexer to substantially mimic characteristics of an output driver in the flip flop.

With respect to claim 15, Chen et al. discloses, in Figure 7, a first input [D] coupled to drive a first transmission gate [66,68,70,72], and a second input [Db] coupled to drive a second transmission gate [74,76,78,80], the multiplexer further including a select input coupled to the clock source [CLK2, CLK2b] to selectively enable one of the transmission gates, wherein the output is coupled to the first and second transmission gates and the transmission gates are configured to correspond substantially to slave transmission gates in a flip-flop.

With respect to claim 17, Chen et al. discloses, in Figure 7, an inverter [84] coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.

With respect to claim 21, Oosera et al. discloses, in Figure 1, a) a signal source [10] to generate a signal, b) a signal distribution circuit [12] to modify the signal and distribute a modified signal, and including a flip-flop that introduces a first propagation delay in the modified signal; and b) a delay matching circuit [11] to distribute the signal and introduce a second propagation delay to the signal, the second propagation delay substantially matching the first propagation delay introduced in the modified signal by the flip-flop.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 2, 4, 6, 7, 8, 11, 12, 22-24, 27, 29, 31, 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Oosera et al. (JP. Patent No. JP409046189A) in view of Chen et al. (U.S. Patent No. 6,002,284).

With respect to claims 2, 4, 6, 12 and 29, Oosera et al. discloses all of the claimed limitations as expressly recited in claims 1 and 28, except for the details of the delay matching including a multiplexer having a select line coupled to a clock source, transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop, inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop, and an output coupled to the multiplexer to substantially mimic characteristics of an output driver in the flip flop and the multiplexer includes a select line coupled to the clock source.

Chen et al. discloses, in Fig. 7, a delay matching including a multiplexer having a select line coupled to a clock source, transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop, inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop, and an output coupled to the multiplexer to substantially mimic characteristics of an output driver in the flip flop and the multiplexer includes a select line coupled to the clock source [CLK2,CLK2b].

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the clock distribution circuit of Oosera with a delay matching in the form of a multiplexer to facilitate the required delay to enhance system synchronization since such circuit arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Chen et al.

With respect to claim 7-8, 11, 31 and 33, Oosera et al. discloses all of the claimed limitations as expressly recited in claims 1 and 28, except for the details of the delay matching including a multiplexer having a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the clock source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, in which the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop, the transmission gates are configured to correspond substantially in size to the slave transmission gate in the flip-flop, and an inverter coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.

Chen et al. discloses, in Fig. 7, a delay matching including a multiplexer having a first input [D] coupled to drive a first transmission gate [66,68,70,72], a second input [Db] coupled to drive a second transmission gate [74,76,78,80], a select input coupled to the clock source [CLK2, CLK2b] to selectively enable one of the transmission gates, and an output [input to 84] coupled to the first and second transmission gates, in which the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop, the transmission gates are configured to correspond substantially in size to the slave transmission gate in the flip-flop, an inverter coupled to the output of the multiplexer, wherein the inverter is configured to correspond substantially to an output driver in the flip flop.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the clock distribution circuit of Oosera with a delay matching in the form of a

multiplexer to facilitate the required delay to enhance system synchronization since such circuit arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Chen et al.

With respect to claims 22-24 and 27, Oosera et al. discloses all of the claimed limitations as expressly recited in claim 21, except for the delay matching circuit includes a multiplexer having a select line coupled to a signal source; transmission gates within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop; inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop; and an output coupled to the multiplexer to substantially mimic characteristics an output driver in the flip flop; a first input coupled to drive a first transmission gate, a second input coupled to drive a second transmission gate, a select input coupled to the signal source to selectively enable one of the transmission gates, and an output coupled to the first and second transmission gates, wherein the transmission gates are configured to correspond substantially to a slave transmission gate in the flip-flop; the transmission gates are configured to correspond substantially in size to the slave transmission gate in the flip-flop.

Chen et al. discloses, in Figure 7, a multiplexer having a select line coupled to a clock source [CLK2, CLK2b], transmission gates [(66,68,70,72); (74,76,78,80)] within the multiplexer to substantially mimic characteristics of a slave transmission gate in a flip-flop, inputs coupled to the multiplexer to substantially mimic characteristics of a master output driver of the flip-flop, and an output coupled to the multiplexer to substantially mimic characteristics of an output driver in the flip flop, a select line coupled to the clock source [CLK2,CLK2b], a first input [D]

coupled to drive a first transmission gate [66,68,70,72], and a second input [Db] coupled to drive a second transmission gate [74,76,78,80], the multiplexer further including a select input coupled to the clock source [CLK2,CLK2b] to selectively enable one of the transmission gates, wherein the output is coupled to the first and second transmission gates and the transmission gates are configured to correspond substantially to slave transmission gates in a flip-flop.

It would have been obvious to one of ordinary skill in the art at the time of the invention to configure the clock distribution circuit of Oosera with a delay matching in the form of a multiplexer to facilitate the required delay to enhance system synchronization since such circuit arrangement of the logic circuit for the stated purpose has been a well known practice as evidenced by the teachings of Chen et al.

Allowable Subject Matter

10. Claim 20 is allowed.

11. Claims 9-10, 16, 25-26 and 32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter.

The closest prior art on record does not show or fairly suggest:

A delay matching circuit including a PMOS transistor having a drain coupled to the first input, a gate coupled to ground, and a source coupled to a supply voltage, wherein the PMOS transistor is configured to correspond substantially to a PMOS transistor in a master output driver of the flip-flop; and b) an NMOS transistor having a drain coupled to the second input, a gate coupled to the supply voltage, and a source coupled to ground, wherein the NMOS transistor is

configured to correspond substantially to an NMOS transistor in the master output driver of the flip-flop, as called for in claims 9, 16, 20 and 25.

Citation of Relevant Prior Art

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Prior art Morley (U.S. Patent No. 5,774,080) discloses a reduced transistor-count storage and multiplexing system.

Prior art Lofgren (U.S. Patent No. 4,797,575) discloses a flip-flop with identical propagation delay in clock pass through mode and in normal operation.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linh M. Nguyen
Examiner
Art Unit 2816

LMN